Clock Synchronization UNIT (CSU)* Datasheet

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Features

- Clock synchronization by means of automatic variation of the duration between two clock ticks
- Programmable correction of clock state and clock rate
- Two state registers with different resolutions ($1\mu s$ and $100\mu s$) available
- Programmable output interrupt mode and period
- Sample and hold register for the accurate determination of an interrupt signal (e.g. arrival time of an incoming message)
- DMA compatible interface, such that the CSU registers can be accessed with a memory fetch operation (e.g. in order to timestamp an outgoing message)
- Programmable timeout support
- Processor independent peripheral device
- 16 bit databus
- Single 5V power supply
- 28 pin dual-in-line package

*The CSU is produced by Austria Mikro Systeme International GmbH with the chip number "S65C60".

Applications

- Realization of a logical clock whose state can be corrected and rate can be readjusted
- Efficient implementation of a fault-tolerant global time base by synchronization of the local clocks of each node in a distributed system
- Measurement of accurate arrival times of events

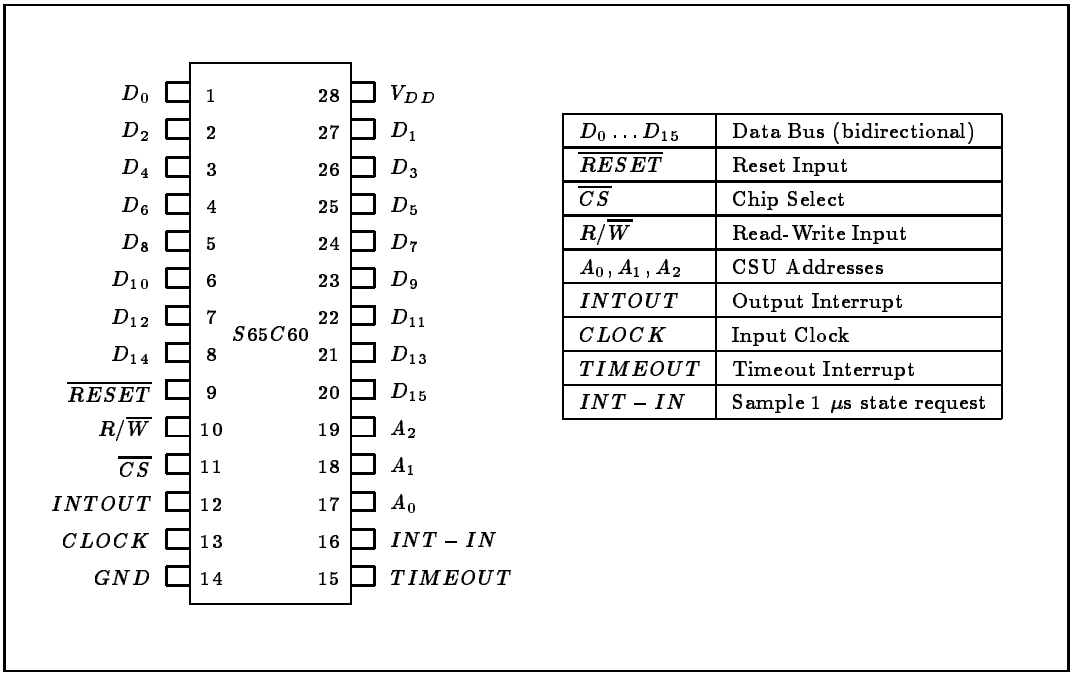
General Description

The Clock Synchronization Unit (CSU) is a peripheral device for 16 bit microprocessor. It is produced in a 28 pin dual-in-line package (see figure 1).

The objectives of the CSU are:

- to provide a global time reference in a distributed real-time computer system
- to improve the synchronization accuracy
- to reduce the CPU load for clock synchronization

The CSU (see figure 2) provides a high resolution register with a granularity of $1\mu s$ and a low resolution register with a granularity of $100\mu s$.



$D_0 \ldots D_{15}$	Data Bus (bidirectional)
$\overline{RESET}$	Reset Input
$\overline{CS}$	Chip Select
$R/\overline{W}$	Read-Write Input
A_0, A_1, A_2	CSU Addresses
$INTOUT$	Output Interrupt
$CLOCK$	Input Clock
$TIMEOUT$	Timeout Interrupt
$INT-IN$	Sample 1 μs state request

Figure 1: Pin Configuration

It contains the correction logic for the continuous correction of the clock state and the clock rate. The CSU enables the CPU to sample the state (time stamp) of the high resolution ($1\mu s$) state register. Furthermore, the CSU is able to monitor the interrupt line (*INT-IN*) and to store the $1\mu s$ state register content at the occurrence of the active edge of an interrupt.

The CSU provides a fully programmable (mode and period) output signal (interrupt output) which can be used as interrupt signal for the CPU. In order to improve the observation of time dependent operation, e.g. device polling, message passing via TDMA protocols, etc., a debug option is available. In this mode all outputs can be reduced in speed by a programmable factor for a programmable time interval. Additionally the CSU provides a fully programmable (countdown speed and output mode) timeout counter.

The accuracy of the content of the state register for time determinations is defined by the CSU input clock. This input clock can be derived from the system clock or from any other frequency standard. Thus CPU and CSU can operate asynchronously.

Detailed Description

The CSU has 8 read registers and 8 write registers (see figure 3) which can be selected by three 3 address lines (A_0, A_1, A_2) and by the $R/\overline{W}$ line. Besides the *power supply* (V_{DD}), the *ground* (GND) and the *clock* ($CLOCK$) line there are three control lines ($\overline{RESET}$, $\overline{CS}$, $INT-IN$) and two output lines ($INTOUT$, $TIMEOUT$) which will be described below. (See figure 1 for the pin configuration of the CSU chip).

Writing to register R_0 acts as a software reset of the CSU. A software reset resets the entire CSU except the rate correction register R_5 (see below) which is cleared only by an active hard-

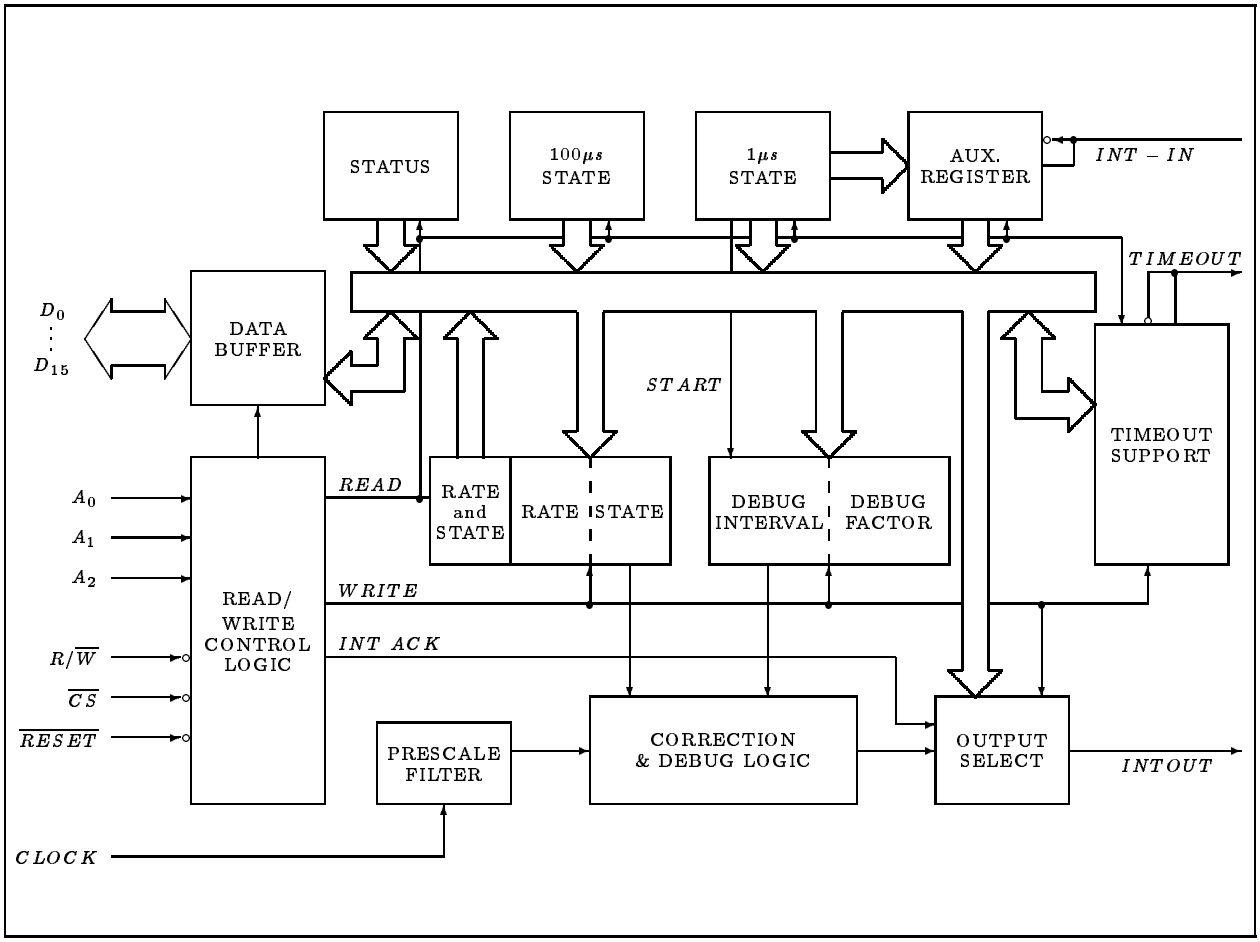


Figure 2: Block Diagram

ware reset signal ($\overline{RESET}$) or by a simple write of zero to this register by the CPU.

$D_0 \ldots D_3$ of register R_0 contain the operating frequency of the CSU in MHz. If $D_4 = high$ the input clock rate is divided by 2, otherwise the input clock rate is not affected. The state of $D_5 \ldots D_{15}$ do not care. The operating frequency definition is used in the prescale-filter (see the block diagram of the CSU in figure 2) to obtain an internal clock rate of 1 MHz which corresponds to a clock period of $1\mu s$. This clock is used for the high resolution state register counter R_1 and thus determines the resolution of measurements.

As described below the mode register R_7 is used in different functions of the CSU to set the suitable parameters. In order to work correctly $D_{10} \ldots D_{15}$ of register R_7 should always be set to low.

The high resolution state register R_1 ($1\mu s$) has a length of 20 bits and the low resolution state register R_3 ($100\mu s$) has a length of 14 bits. These 14 bits ($D_0 \ldots D_{13}$) of the low resolution state register can be read by a single operation. D_{14} and D_{15} are always set to low. In order to read the 20 bit high resolution state registers, two read operations are necessary. Therefore, when reading the least significant bits of

	A_2	A_1	A_0	READ($R/\overline{W} = high$)	WRITE($R/\overline{W} = low$)
R_0	0	0	0	STATUS and MSBits $1\mu s$	frequency and soft reset
R_1	0	0	1	$1\mu s$ STATE	DEBUG factor
R_2	0	1	0	STATUS and MSBits $1\mu s$	DEBUG duration
R_3	0	1	1	$100\mu s$ STATE	STATE correction
R_4	1	0	0	TIMEOUT	TIMEOUT
R_5	1	0	1	RATE & STATE correction	RATE correction
R_6	1	1	0	TIMESTAMP	output interrupt acknowledge
R_7	1	1	1	STATUS and MSBits timestamp	MODE register

Figure 3: Read and Write Registers of the CSU

the high resolution register ($D_0 \ldots D_{15}$ of register R_1), the four most significant bits are copied to an auxiliary register and can be accessed in a second read operation by reading $D_0 \ldots D_3$ of the status register R_0 or R_2. Therefore each double read operation of the $1\mu s$ state register is atomic. The goal of the double addressing for the status register R_0 and R_2 is to enable flexible up and down burst read operations for DMA devices.

State and Rate Correction

Clock drifts are caused by physical crystal Quartzes with frequencies deviating from the nominal frequency by degradation or maladjustment. In order to synchronize the CSU mutually with other clocks, state and rate correction can be applied. The rate correction can be used for continual correction of stationary deviations (systematic rate errors of the individual clock, e.g. rate errors caused by mechanical imprecision of the quartz crystal) in $\mu s/s$ and the state correction can be used for unique corrections in μs.

The sum of the corrections has to be in the range of $\pm 2^{15} \mu s/s$ in steps of $1\mu s/s$. Corrections are made by equidistant insertions or suppressions of input clock pulses during a synchronization interval of $0,5s$. Therefore, the state registers are monotonically incremented at all events. If the maximum clock correction is used, then the maximum error for interval measurements is $6,2\%$ for intervals up to $16\mu s$ and $3,2\%$ for intervals up to $1s$. The correction is performed by a special prescale-filter with an output clock-rate of nominally 1 MHz which is used as input clock for the counter of the high resolution state register. This high effort is necessary to ensure that time stamps are consistently sampled in the network even during synchronization intervals.

The correction of the clock state and clock rate is supported by two registers, the state and the rate correction register. A rate correction value can be written to register R_5 and causes a periodical correction of the input clock rate. In this way the deviation of the internal clock rate of a nominal mean value can be brought down to 1 ppm ($1\mu s/s$). This error, however, causes an increasing deviation of the state register count from the desired nominal value. It can be corrected by writing the time difference to register R_3. The form for the correction value is shown in figure 4.

The maximum time correction (sum of register R_3 and register R_5) is $\pm 32768\mu s/s$. The programmer should always limit the sum of rate and state correction values to this maximum value, otherwise the CSU issues an overflow in the status information.

The actual correction value (sum of state and rate correction) can be accessed by the CPU by reading register R_5. At the beginning of each synchronization interval the actual correction value is computed and stored in this register. By writting the state correction to register R_3 a special status flag in the registers R_0, R_2 and R_7 is set. The status flag is reset at the beginning of the synchronization interval indicating

Correction Registers R_3 and R_5																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Carry	Sign	Rate Correction ($\mu s/s$) State Correction (μs)														

Figure 4: Correction Registers

that the next state correction can be entered.

Part of Mode Register R_7 (see Fig. 9)				
D_3	D_2	D_1	D_0	Interval
0	X	X	X	No Interval Redefinition
1	0	0	0	$125\mu s$
1	0	0	1	$250\mu s$
1	0	1	0	$500\mu s$
1	0	1	1	$1ms$
1	1	0	0	$2ms$
1	1	0	1	$4ms$
1	1	1	0	$8ms$
1	1	1	1	$1s$

Figure 5: Interrupt Out Interval

Part of Mode Register R_7 (see Fig. 9)		
D_9	D_8	Description
0	X	No Mode Redefinition
1	0	Strobe Mode
1	1	Static Mode

Figure 6: Interrupt Out Mode

Programmable Output Interrupt

The CSU provides a fully programmable (mode and period) output signal (interrupt output) ($INTOUT$). This output signal can be used as an interrupt signal for the CPU. The interval of this output signal is defined by a single write operation to the mode register R_7 (figure 9). Values can be selected in 8 steps from $125\mu s$ up to $1s$ by bits $D_0 \ldots D_3$ of register R_7 (see figure 5). The selected status can be read in one of the partially redundant status registers R_0, R_2 or R_7 (see figure 7). The operation mode of the output signal can be defined by bit D_8 of the mode register R_7 as shown in figure 6. In strobe mode the CSU generates a periodical output signal with a pulse width of approximately $1\mu s$. In static mode the periodically generated signal has to be acknowledged by a single write operation to register R_6 in order to be reset by the CSU.

Time-Stamp Feature

For clock synchronization, the CSU is able to monitor the interrupt line ($INT - IN$) and to copy the content of the $1\mu s$ state register R_1 into a time stamp register at the occurrence of the active edge of an interrupt. The LSBits (least significant bits) $D_0 \ldots D_{15}$ of the time stamp register can be accessed via register R_6, the MSBits (most significant bits) $D_{16} \ldots D_{19}$ can be accessed as $D_0 \ldots D_3$ from register R_7. The polarity of the active edge can be defined in the mode register R_7 by D_6 (figure 9). If $D_6 = low$ the positive edge of the interrupt signal is active, otherwise the negative one is active. The sampled value remains stored until it is overwritten at the next interrupt.

Timeout Counter

The CSU provides a fully programmable (countdown speed and output mode) timeout counter. This built-in timeout counter shows an optimal hardware-software interface. Countdown speed and output signal mode are fully programmable by means of the content of the mode register R_7 (figure 9). The timeout countdown is started by a write operation to register R_4. The timeout period is determined by the value written to register R_4 times the speed reduction factor in debug mode times a basic time interval. The basic time interval is determined by bit D_5 of

Status Registers R_0, R_2 and R_7			
Bit(s)			Flag Description
$D_0 \ldots D_3$			MSBits of $1\mu s$ State and Timestamp Register
D_6	D_5	D_4	Output Signal Interval
0	0	0	$125\mu s$
0	0	1	$250\mu s$
0	1	0	$500\mu s$
0	1	1	$1ms$
1	0	0	$2ms$
1	0	1	$4ms$
1	1	0	$8ms$
1	1	1	$1s$
$D_7 \ldots D_{10}$			Operating Frequency $(4 - 12\text{MHz})$
$D_{11} = low$			Input Clock not Affected
$D_{11} = high$			Input Clock Divided by 2
$D_{12} = high$			Rate and State Correction Overflow
$D_{13} = low$			Debug Mode off
$D_{13} = high$			Debug Mode on
$D_{14} = low$			Timeout is Signalled at Pin 15
$D_{14} = high$			No Timeout is Signalled
D_{15}			Not used

Figure 7: Status Register Bit Assignment

the mode register R_7. If $D_5 = low$ the basic time interval is $100\mu s$, otherwise ist is $1\mu s$.

The timeout counter can be stopped by a read operation on register R_4. In this case the content of register R_4 defines the remainder of the timeout interval. If the timeout interval elapses, an interrupt signal is generated ($TIMEOUT$). This interrupt will be reset by a single read or write operation to the timeout register R_4. The active state of this signal is defined by D_4 of the mode register R_7. If $D_4 = low$ the interrupt signal is active high, otherwise it is active low.

It should be considered, that after reset the timeout signal on pin $TIMEOUT$ is passive high.

Debug Option

In order to increase the observability of time dependent operations, e.g. device polling, message passing via TDMA (Time Division Multiple Access) protocols, etc., a debug option is available. This feature enables the programmer to reduce the speed in all nodes of a distributed real time system at the same time for the same duration.

In debug mode, all outputs (states and interrupts) are reduced in speed by a programmable factor (10, 100, 1000, 10000) for a programmable interval (up to 2^{14} ticks). Before entering the debug mode it is necessary to set the debug reduction factor and the debug duration. The speed reduction factor can be defined by a write operation to register R_1 in the format shown in figure 8. This write operation has to be performed prior to definitions of a debug interval since the speed reduction factor will not be predefined by resets and thus is not initialized. Entering the debug mode is evoked by writing the debug interval to register R_2. The CSU starts the debug mode at the beginning of a synchronization interval. The debug interval is determined by bits $D_0 \ldots D_{15}$ and is given in μs times the speed reduction factor with respect to the physical time.

Part of Mode Register R_7 (see Fig. 9)			
D_1	D_0	Speed Reduction Factor	
0	0	10	$D_2 \ldots D_{15}$ don't care
0	1	100	
1	0	1000	
1	1	10000	

Figure 8: Debug Factor

Electrical and Timing Characteristics

The CSU contains circuits to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. See figure 14 for the absolute maximum ratings. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Additionally different electrical and timing conditions have to be kept. The conditions for the input clock can be seen in figures 12 and 11. The detailed values are shown in figure 13.

In figure 10 the timing diagram which have to be satisfied for correct reading and writing the registers of the CSU is described and the exact values are shown in figure 13 too.

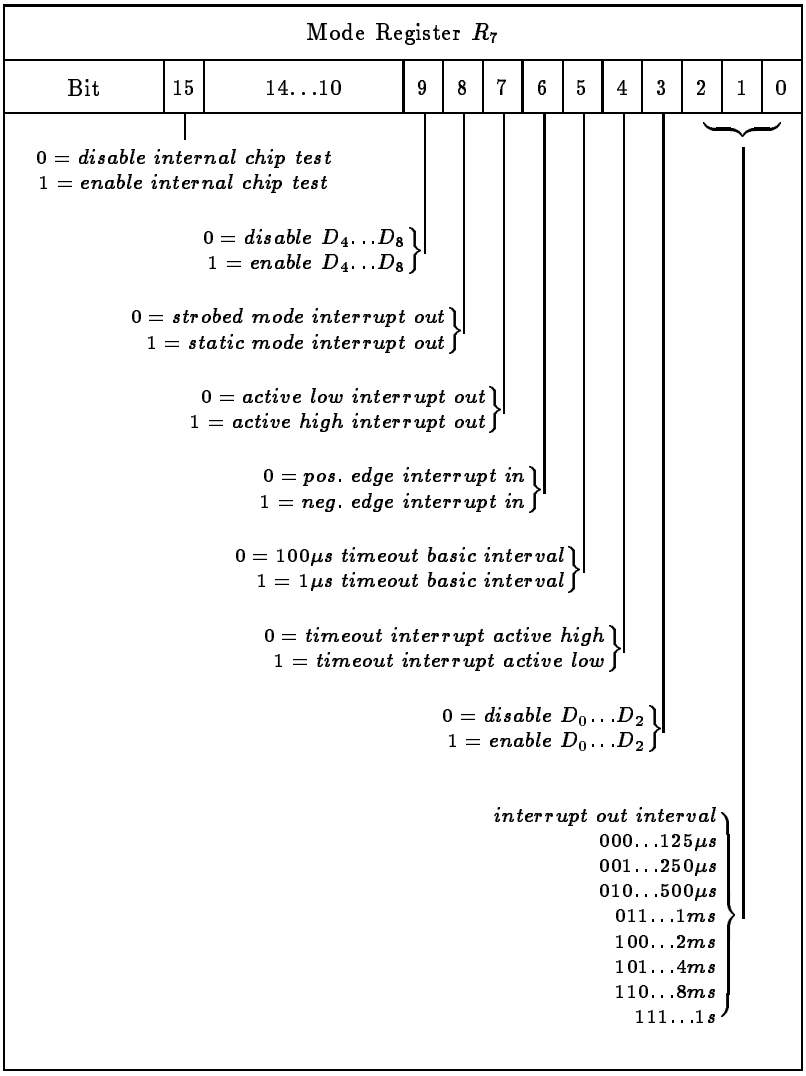


Figure 9: Mode Register Bit Assignment

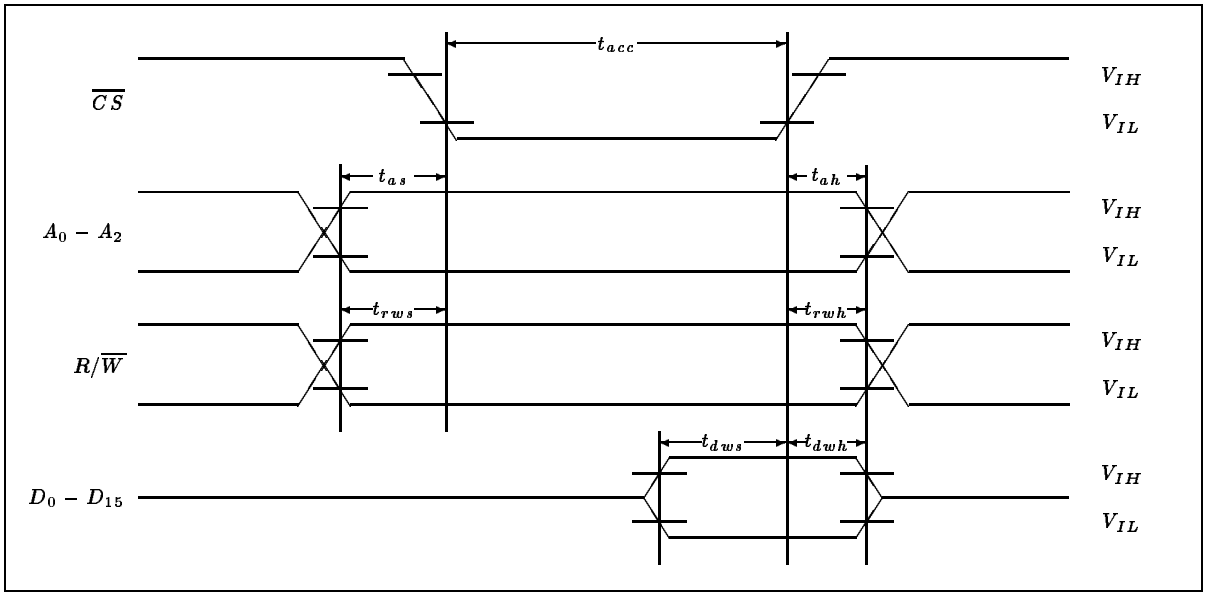


Figure 10: Read-Write Timing Characteristics

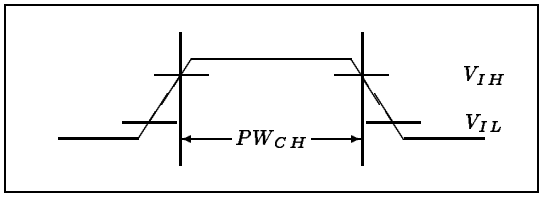


Figure 11: Clock Pulse Width, High-State

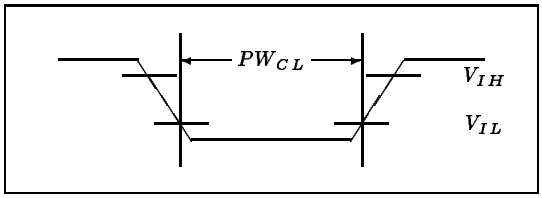


Figure 12: Clock Pulse Width, Low-State

Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	4.75	5	5.25	V
T_A	Operating Temperature	0	25	70	°C
V_{IH}	Input High Voltage	$70\%V_{DD}$		V_{DD}	V
V_{IL}	Input Low Voltage	0		$30\%V_{DD}$	V
I_{IN}	Input Leakage Current (Except D_0 – D_{15})	-1	.001	$+1$	μA
I_{TSI}	TriState Input Current (D_0 – D_{15})	-10	.01	$+10$	μA
V_{OH}	Output High Voltage (sourcing 1mA)	$V_{DD} - 0.5$			V
V_{OL}	Output Low Voltage (sinking 1mA)			0.5	V
P_D	Power Dissipation (Outputs unloaded)		5	20	mW
C_{IN}	Input Capacitance		7		pF
C_{TS}	TriState Capacitance ($D_0 - D_{15}$)		7		pF
C_{OUT}	Output Load Capacitance		12		pF
PW_{CL}	Minimum Clock Pulse Width, Low (Fig. 12)	35			nS
PW_{CH}	Minimum Clock Pulse Width, High (Fig. 11)	35			nS
f_c	Clock Frequency	4		12	MHz
t_{acc}	Access Time (Fig. 10)	150			nS
t_{as}	Address Setup Time (Fig. 10)	10			nS
t_{ah}	Address Hold Time (Fig. 10)	10			nS
t_{dws}	Data Write Setup Time (Fig. 10)	120			nS
t_{dwh}	Date Write Hold Time (Fig. 10)	0			nS
t_{rws}	Read/Write Setup Time (Fig. 10)	10			nS
t_{rwh}	Read/Write Hold Time (Fig. 10)	10			nS

Figure 13: Electrical Operating Characteristics ($V_{SS}/GND = 0V$)

Supply Voltage (V_{DD} – V_{SS}) ..... -0.5V to $+7.0$V
Input Voltage ..... $V_{SS} - 0.5$V to $V_{DD} + 0.5$V
Operating Temperature Range ..... 0°C to $+70°$
Storage Temperature Range ..... -65°C to $+150°$

Figure 14: Absolute Maximum Ratings